8086/8088 Instruction Execution Times

The following symbols are used to refer to instruction operands:

regd	- 8 or 16 bit register, destination
regs	- 8 or 16 bit register, source
sreg	- segment register
mem	- memory location as either source or destination
acc	- 8 or 16 bit accumulator (AL or AX)

Arithmetic and Logical Instructions

Instruction	Clock Cycles	Transfers
General Arithmetic and Logical Instructions		
ADD		
ADC		
SUB		
SBB		
CMP		
AND		
OR		
XOR		
TEST		
regd,regs	3	
regd,mem	9+EA	1
mem,regs	16+EA	2
regd,imm	4	1
mem,imm	17+EA	2
acc,imm	4	
Negation Instructions		
NEG		
NOT		
reg	3	
mem	16+EA	2
Increment and Decrement Instructions		
INC		
DEC		
8 bit reg	3	
16 bit reg	2	
mem	15+EA	2
Miscellaneous Arithmetic Instructions		
CBW	2	
CWD	5	

Instruction	Clock Cycles	Transfers
Shift and Rotate Instructions		
SAL/SHL		
SHR		
SAR		
ROL		
RCL		
ROR		
RCR		
reg (1 bit shift)	2	
mem (1 bit shift)	15+EA	2
reg (multi-bit shift)	8+4/bit	
mem (multi-bit shift)	20+EA+4/bit	2
Multiplication and Division Instructions		
DIV		
8 bit reg	80-90	
16 bit reg	144-162	
8 bit mem	86-96 + EA	
16 bit mem	171-190 + EA	1
IDIV		
8 bit reg	101-112	
16 bit reg	165-184	
8 bit mem	107-118 + EA	
16 bit mem	171-190 + EA	1
MUL		
8 bit reg	70-77	
16 bit reg	118-133	
8 bit mem	76-83 + EA	
16 bit mem	124-139 + EA	1
IMUL		
8 bit reg	80-98	
16 bit reg	128-154	
8 bit mem	86-104 + EA	
16 bit mem	134-160 + EA	1
Decimal Operations		
AAA	4	
AAD	60	
AAM	83	
AAS	4	
DAA	4	
DAS	4	

Data Transfer Instructions

Instruction	Clock Cycles	Transfers
Move Instructions		
MOV		
acc,mem	10	1
mem,acc	10	1
regd,regs	2	
regd,mem	8+EA	1
mem,regs	9+EA	1
reg,imm	4	1
mem,imm	10+EA	1
sreg,regs	2	
regd,sreg	2	
sreg,mem	8+EA	1
mem,sreg	9+EA	1
Stack Operations		
PUSH		
reg	11	1
mem	16+EA	2
sreg	10	1
POP		
reg	8	1
mem	16+EA	2
sreg	8	1
PUSHF	10	1
POPF	8	1
I/O Instructions		
IN		
Fixed port	10	1
Variable port (DX)	8	1
OUT		
Fixed port	10	1
Variable port (DX)	8	1
Misc. Data Transfer Instructions		
XCHG		
reg,acc or acc,reg	3	
reg,reg	4	
reg,mem or mem,reg	17+EA	2
LAHF	4	
SAHF	4	
XLAT	11	
LEA	2+EA	
LDS	16+EA	2
LES	16+EA	2

Control Transfer Instructions

Instruction	Clock Cycles	Transfers
Unconditional Jump Instruction		
JMP		
Intrasegment direct short	15	
Intrasegment direct	15	
Intersegment direct	15	
Intrasegment mem-indirect	18+EA	1
Intrasegment reg-indirect	11	
Intersegment mem-indirect	24+EA	2
Conditional Jump Instructions		
JA / JNBE	16/4	
JAE / JNB / JNC	16/4	
JB / JNAE / JC	16/4	
JBE / JNA	16/4	
JCXZ	16/4	
JE / JZ	16/4	
JG / JNLE	16/4	
JGE / JNL	16/4	
JL / JNG	16/4	
JLE / JNG	16/4	
JNE / JNZ	16/4	
JNO	16/4	
JNP / JPO	16/4	
JNS	16/4	
JO	16/4	
JP / JPE	16/4	
JS	16/4	
Loop Instructions		
LOOP	17/5	
LOOPE / LOOPZ	18/6	
LOOPNE / LOOPNZ	19/7	
Call and Return Instruction		
CALL		
Intrasegment direct	19	1
Intersegment direct	28	2
Intrasegment mem-indirect	21+EA	2
Intrasegment reg-indirect	16	1
Intersegment mem-indirect	37+EA	4
RET		
Intrasegment	16	1
Intrasegment with pop	20	1
Intersegment	18	2
Intersegment with pop	26	2

Interrupt Instructions		
INT (other than INT 3)	52	5
INT 3	51	5
INTO		
Taken	53	5
Not Taken	4	
IRET	24	3
INTR		
(hardware interrupt request)	61	7
NMI		
(nmi interrupt request)	50	5

String Instructions

Instruction	Clock Cycles	Transfers
CMPS / CMPSB / CMPSW		
Not Repeated	22	2
Repeated	9+22/rep	2/rep
LODS / LODSB / LODSW		
Not repeated	12	1
Repeated	9+13/rep	1/rep
MOVS / MOVSB / MOVSW		
Not Repeated	18	2
Repeated	9+17/rep	2/rep
SCAS / SCASB / SCASW		
Not Repeated	15	1
Repeated	9+15/rep	1/rep
STOS / STOSB / STOSW		
Not Repeated	11	1
Repeated	9+11/rep	1/rep

Miscellaneous and Processor Control Instructions

Instruction	Clock Cycles	Transfers
CLC	2	
CLD	2	
CLI	2	
CMC	2	
STC	2	
STD	2	
STI	2	
NOP	3	
REP	2	
REPZ / REPE	2	
REPNZ / REPNE	2	

Effective Address Calculation Times

Addressing Mode	Clock Cycles
Displacement only	6
Base or Index	5
Displacement + Base or Index	9
Base + Index	
BP+DI or BX+SI	7
BP+SI or BX+DI	8
Displacement + Base + Index	
BP+DI+disp or BX+SI+disp	11
BP+SI+disp or BX+DI+disp	12